SYZYGY®

SYZYGY Specification

Version 1.1

Revision History:

Date	Version	Description
2017-08-07	1.0	Initial release.
2018-04-20	1.0.1	Removed the R_GA table and instead refer to the SYZYGY DNA Specification 1.0.
2019-07-15	1.1	Added TXR-4 transceiver peripheral specification. TXR transceiver peripheral of the original 1.0 version has been renamed TXR-2. Added a note to Table 6 that "Peripherals should connect unused pins to ground." Added a note to Table 6 that "Peripherals should leave these pins unconnected if not used." Added a note about AC-coupling to transceiver signal descriptions. Additional formatting updates to aid navigation and reading and typo fixes. Additional requirement added for peripherals to prevent driving I/O until VIO is up.

Contents

1. Introduction

SYZYGY® is an open standard for connecting high performance peripherals to FPGA systems using a commodity connector and common electrical specification. This document contains the official specification for the SYZYGY standard. Additional companion documentation is available for carrier and peripheral designers at the link below:

https://docs.opalkelly.com/display/SZG/SYZYGY

1.1. Overview

SYZYGY was created to fill the cost and performance gap between existing peripheral standards such as Digilent PMOD and FMC (VITA 57.1). Although not specifically required, this standard is most applicable to FPGA-based carriers.

SYZYGY advantages:

- Supports high-speed single-ended and differential signaling up to 25 Gbps
- Utilizes compact, high-density connectors for small, single-purpose peripherals
- Facilitates wired remote peripherals using cable-compatible connectors
- Enables low-cost assembly using commodity SMD technologies

SYZYGY target peripherals:

- High speed data acquisition (ADC)
- High speed DAC
- Image capture
- Software-defined radio
- Video input and output
- Multi-channel I/O
- Digital communications
- SYZYGY target applications:
- High performance prototypes
- Evaluation systems for high-performance semiconductors
- Systems integration and testing

1.2. Features

The SYZYGY specification defines three types of peripherals: standard, transceiver TXR-2, and transceiver TXR-4.

Standard SYZYGY features:

- 40-pin 0.8mm Samtec connector
- 5V, 3.3V fixed voltages
- Programmable VIO supply
- MCU for peripheral personality and VIO setting
- 8 differential pairs (or 16 single-ended signals)
- 12 additional single-ended signals

- Dedicated clock inputs/outputs

Transceiver SYZYGY features:

- 40-pin 0.5mm Samtec connector
- 5V, 3.3V fixed voltages
- Programmable VIO supply
- MCU for peripheral personality and VIO setting
- 18 additional single-ended signals
- Dedicated clock inputs / outputs
- TXR-2 ports have 4 transceiver pairs and reference clock for high-performance I/O
- TXR-4 ports have 8 transceiver pairs and reference clock for high-performance I/O

1.3. Terminology

Table 1: Transceiver Pod Dimensions

Term	Definition
carrier	The host-side component in an SYZYGY system. A carrier includes a host, a system controller, a power supply system, and one or more ports.
host	The semiconductor device to which pod I/O are connected to on a carrier. Typically an FPGA.
SmartVIO controller	The I²C master for all ports on a carrier. Manages VIO configuration.
pod	A peripheral component in an SYZYGY system. A pod connects to a port on a carrier. A pod may be one of three types: standard, transceiver TXR-2, or transceiver TXR-4.
port	A socket on a carrier for connecting a pod. Ports may be one of three types: standard, transceiver TXR-2, or transceiver TXR-4.
standard pod/port	An interface type which supports single-ended and differential pair I/O over a 40-pin connector.
transceiver pod/port	An interface type which supports single-ended and differential pair transceiver I/O over a 40-pin connector with differential pair spacing. This term generally applies to both TXR-2 and TXR-4 unless otherwise specified.
single-wide pod	A pod which utilizes one port on a carrier.
double-wide pod	A pod which utilizes two adjacent ports of the same type on a carrier.
VIO group	A group of ports on a carrier which share the same VIO power supply rail.
pMCU	The peripheral microcontroller unit. Each pod includes a pMCU with non-volatile memory for storage of hardware parameters, communicated to the SmartVIO controller over I²C.
SmartVIO	A means of automatically configuring the VIO voltage for a VIO group using the hardware parameters of the pods connected to that group.
P2C	Denotes the directionality of a clock or data signal which originates at the pod and terminates at the carrier.
C2P	Denotes the directionality of a clock or data signal which originates at the carrier and terminates at the pod.

1.4. System Components

The SYZYGY system consists of two main components: carriers and pods. The carrier integrates a host, a SmartVIO controller, and power supply rails for one or more pods. Three types of pods are defined: standard, transceiver TXR-2, and transceiver TXR4. A pod connects to a port of the same type on the carrier, either by direct board-to-board mating or by cable.

1.4.1. System Block Diagram
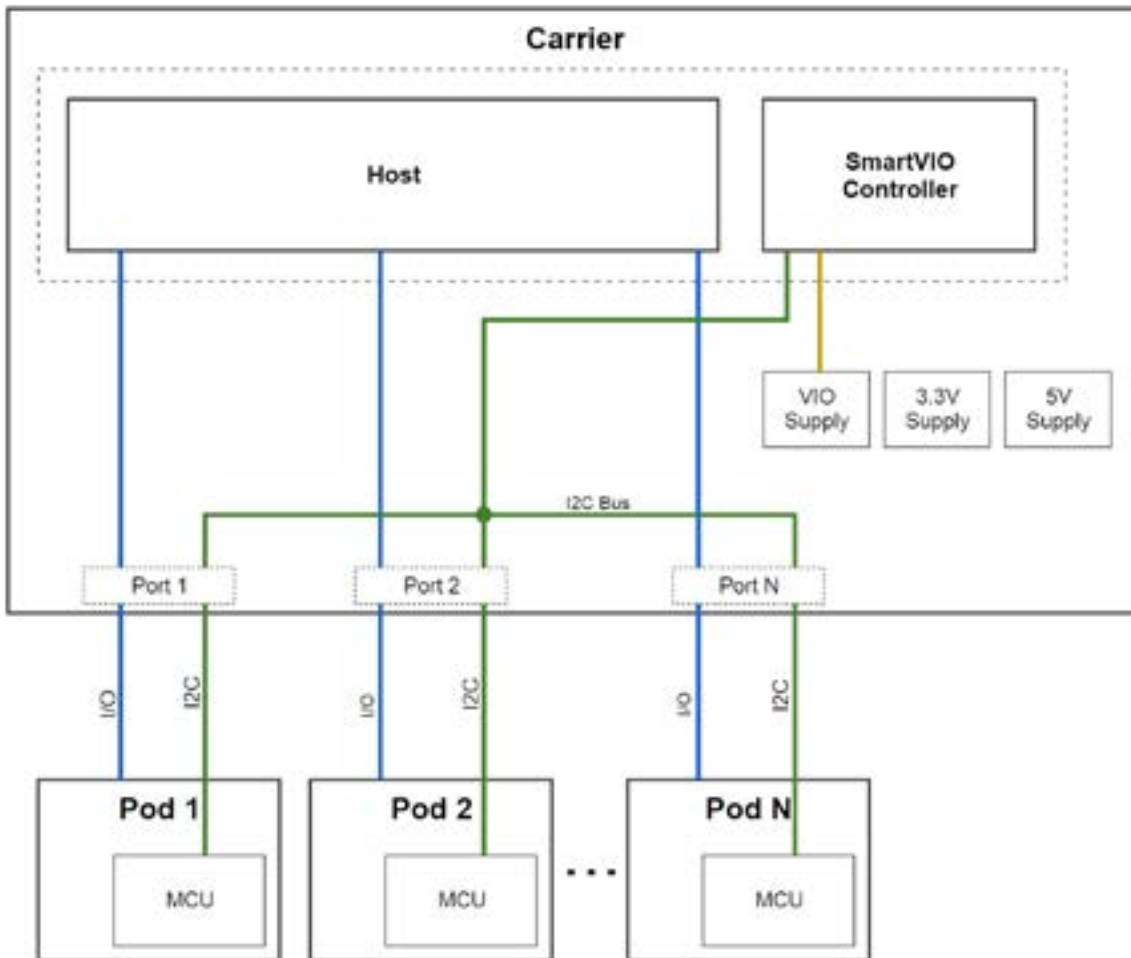
Figure 1. SYZYGY System Block Diagram

1.4.2. Carrier

A carrier includes three functions: a host, power supplies for peripherals, and a SmartVIO controller. The host is the I/O endpoint for the pods connected to the carrier and is expected to be an FPGA. The SmartVIO controller may be separate or integrated with the host (an FPGA with an integrated system-on-chip, for example).

A carrier includes one or more ports for connecting pods. Three types of ports are defined: standard, transceiver TXR-2, and transceiver TXR4. A pod may plug directly into a port on a carrier board, or it may be connected by a cable. Ports are separated into VIO groups, and each VIO group is assigned a single VIO voltage which is auto-matically configurable by the SmartVIO controller.

The SmartVIO controller serves as the I²C master for all connected pods. At startup, the controller retrieves the hardware definition stored in the non-volatile memory of the MCU on each connected pod. The controller then configures VIO using a voltage that is compatible with all pods within the group.

1.4.3. Pod

A pod is a peripheral component that attaches to a carrier via a port. Three types of pods are defined: standard, transceiver TXR-2, and transceiver TXR4. While the three types are similar in pinout and form factor, transceiver pods include dedicated transceiver connections to the host and a special connector type with differential pair spacing for increased isolation between pairs.

Mechanically, each pod type has a defined width, but there is no requirement for the length of a pod or its stand-off height when mounted directly to a carrier board.

A standard pod supports single-ended and differential I/O over a 40-pin connector with 0.8-mm pitch. The width of a standard pod is 45 mm.

A transceiver pod supports single-ended and differential transceiver I/O over a 40-pin connector with 0.5-mm pitch and differential pair spacing (every third pin position unused). The width of a transceiver pod is 50 mm.

A pod must include an MCU with non-volatile storage used for storing a set of parameters which describe the pod's functionality and VIO requirements. When connected to a carrier, these parameters are read by the Smart-VIO controller and are used for configuring system parameters such as VIO voltage. See Section 5 for more details.

2. Pinouts and Signal Descriptions

The pod pinout tables below indicate the physical arrangement of the pins along the connector. Standard and transceiver pods both use dual-row connectors with 40 total pin positions (20 per side) plus a center ground spine (not shown in the tables).

The pinout and signal description tables below describe the set of connections available on a fully-populated port. However, some of the signal connections listed are optional and may not be supported on all ports and carriers.

All mentions of transmit (TX) and receive (RX) are relative to the host (i.e. carrier).

A carrier is not required to connect all I/O pins on a port, but the following **I/O Population Rules** must be observed:

1. On standard and transceiver ports, I/O must be filled along the connector in order of pin number. In other words, lower ordinal pin numbers must be connected before higher ordinal pin numbers.
2. On a standard port, signals which are capable of differential I/O must be connected before signals which are single-ended only.
3. On a standard port, only pins 5-20 are considered to be capable of differential I/O signaling.

The following figure shows the orientation of the connector relative to the carrier and the pod boards. In this top-down view, the connector pair is sandwiched between the two boards.

Note: The diagram below shows the recommended placement of a port on the carrier such that the peripheral hangs off the edge of the carrier. Non-edge placement of a port is allowed but carrier manufacturers should provide additional information to customers to help them evaluate peripheral compatibility.
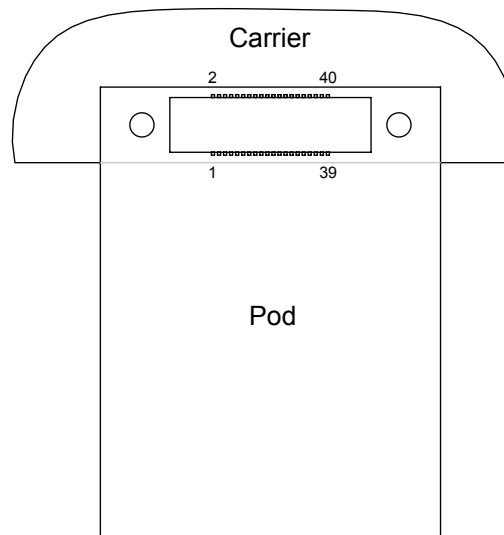
Figure 2. Carrier and Port Orientation with Pin Numbering

2.1. Standard Pod/Port Pinout

Table 2: Standard Pod / Port Pinout

Pin Num	Signal Name	Pin Num	Signal Name
1	SCL	2	+5V
3	SDA	4	R_GA
5	S0_D0P	6	S1_D1P
7	S2_D0N	8	S3_D1N
9	S4_D2P	10	S5_D3P
11	S6_D2N	12	S7_D3N
13	S8_D4P	14	S9_D5P
15	S10_D4N	16	S11_D5N
17	S12_D6P	18	S13_D7P
19	S14_D6N	20	S15_D7N
21	S16	22	S17
23	S18	24	S19
25	S20	26	S21
27	S22	28	S23
29	S24	30	S25
31	S26	32	S27
33	P2C_CLKP	34	C2P_CLKP
35	P2C_CLKN	36	C2P_CLKN
37	RSVD	38	RSVD
39	VIO1	40	+3.3V

2.2. Standard Pod/Port Signal Description

A pod shall not output any signals to the carrier until the VIO supply has been enabled. All pod outputs (including single-ended, differential, clock, and transceiver) must remain at 0 V or in a high-impedance state until VIO has reached a "good" state as determined by the pod. The MCU may be used for the purpose of detecting VIO and gating device outputs or power supplies appropriately to prevent driving outputs into the carrier before VIO is available.

Table 3 below lists the signal groups on the standard port, their direction, and a brief description.

Table 3: Standard Pod / Port Signal Descriptions

Signal Name	Direction	Description
5V	C2P	Fixed 5-V supply, provided by carrier
3.3V	C2P	Fixed 3.3-V supply, provided by carrier
VIO	C2P	I/O supply, provided by carrier
SCL	C2P	I²C clock, provided by SmartVIO controller
SDA	BIDIR	I²C data
R_GA	C2P	Geographical address resistor. See Section 5, "SmartVIO" R_GA is a pulldown to ground on the carrier. The value of R_GA is unique to each port. On the pod, this line is connected to a pullup resistor. The resulting voltage, measuring using an ADC channel on the pMCU, is used to determine the pod's geographical address on the carrier (i.e. I²C address).
D[7:0]{P|N}	BIDIR*	Differential I/O
S[27:0]	BIDIR	Single-ended I/O
P2C_CLK{P|N}	P2C	Differential clock pair provided by pod to carrier. Where possible, these signals should connect to a dedicated clock input on the host.
C2P_CLK{P|N}	C2P	Differential clock pair provided by carrier to pod
RSVD	-	Reserve for future use. Do not connect.

* Due to signal direction limitations on some FPGA devices, a carrier may support only unidirectional differential signaling. Ports on such a carrier must use odd ordinal signal names (e.g. D1P, D1N, D3P, D3N) for RX signals (peripheral to carrier) and even ordinal signal names (e.g. D0P, D0N, D2P, D2N) for TX signals (carrier to peripheral).

2.3. Transceiver Pod/Port Pinout (TXR-2)

A transceiver port is required to connect all transceiver lanes. Single-ended I/O may be partially-populated according to the **I/O Population Rules** above.

Table 4: TXR-2 Transceiver pod / port pinout

Pin Num	Signal Name		Pin Num	Signal Name
1	SCL		2	+5V
3	SDA		4	R_GA
5	RX0P		6	TX0P
7	RX0N		8	TX0N
9	RX1P		10	TX1P
11	RX1N		12	TX1N
13	REFCLKP		14	S0
15	REFCLKN		16	S1
17	S2		18	S3
19	S4		20	S5
21	S6		22	S7
23	S8		24	S9
25	S10		26	S11
27	S12		28	S13
29	S14		30	S15
31	S16		32	S17
33	P2C_CLKP		34	C2P_CLKP
35	P2C_CLKN		36	C2P_CLKN
37	RSVD		38	RSVD
39	VIO1		40	+3.3V

2.4. Transceiver Pod/Port Pinout (TXR-4)

A transceiver port is required to connect all transceiver lanes. Single-ended I/O may be partially-populated according to the **I/O Population Rules** above.

Table 5: TXR-4 Transceiver pod / port pinout

Pin Num	Signal Name
1	SCL
3	SDA
5	RX0P
7	RX0N
9	RX1P
11	RX1N
13	REFCLKP
15	REFCLKN
17	S2
19	S4
21	S6
23	S8
25	RX3P
27	RX3N
29	RX2P
31	RX2N
33	P2C_CLKP
35	P2C_CLKN
37	RSVD
39	VIO1

Pin Num	Signal Name
2	+5V
4	R_GA
6	TX0P
8	TX0N
10	TX1P
12	TX1N
14	S0
16	S1
18	S3
20	S5
22	S7
24	S9
26	TX3P
28	TX3N
30	TX2P
32	TX2N
34	C2P_CLKP
36	C2P_CLKN
38	RSVD
40	+3.3V

2.5. Transceiver Pod/Port Signal Description

A pod shall not output any signals to the carrier until the VIO supply has been enabled. All pod outputs (including single-ended, differential, clock, and transceiver) must remain at 0 V or in a high-impedance state until VIO has reached a "good" state as determined by the pod. The MCU may be used for the purpose of detecting VIO and gating device outputs or power supplies appropriately to prevent driving outputs into the carrier before VIO is available.

A transceiver port is required to connect all transceiver lanes. Single-ended I/O may be partially-populated according to the **I/O Population Rules** above.

Carriers must not include AC-coupling on transceiver lines to ensure compatibility with multiple standards. Peripherals shall provide AC-coupling, as appropriate.

Table 6: Transceiver pod / port signal descriptions

Signal Name	Direction	Description
5V	C2P	Fixed 5-V supply, provided by carrier
3.3V	C2P	Fixed 3.3-V supply, provided by carrier
VIO	C2P	I/O supply, provided by carrier
SCL	C2P	I²C clock for SYZYGY DNA
SDA	C2P	I²C data for SYZYGY DNA
R_GA	C2P	Geographical address resistor. See Section 5, "SmartVIO" R_GA is a pulldown to ground on the carrier. The value of R_GA is unique to each port. On the pod, this line is connected to a pullup resistor. The resulting voltage, measuring using an ADC channel on the MCU, is used to determine the pod's geographical address on the carrier (i.e. I2C address).
RX[3:0]{P|N}	P2C	Transceiver RX pair. These signals must connect to transceiver-capable pins on the host. Peripherals should connect unused pins to ground.
TX[3:0]{P|N}	C2P	Transceiver TX pair. These signals must connect to transceiver-capable pins on the host. Peripherals should leave these pins unconnected if not used.
REFCLK{P|N}	P2C	Transceiver reference clock
S[17:0]	BIDIR	Single-ended I/O
P2C_CLK{P|N}	P2C	Differential clock pair provided by pod to carrier. Where possible, these signals should connect to a dedicated clock input on the host.
C2P_CLK{P|N}	C2P	Differential clock pair provided by carrier to pod
RSVD	-	Reserved for future use

3. Mechanical

A carrier includes one or more ports for attaching pods of various types. A port includes a Samtec mezzanine connector and a pair of mounting holes which are used either for direct board-to-board connection to a pod or attachment via cable. A pod board nominally overlaps the edge of the carrier board by 10 mm.

A standard pod board has a width of 45 mm, and a transceiver pod board has a width of 50 mm. The recommended length for standard and transceiver pods is 70 mm, but a pod may be sized according to the board area needed for the pod design.

The mezzanine connector must be placed centered between the two required mounting holes. These two mounting holes must be positioned as indicated in order to accommodate a compatible Samtec cable.

The four mounting holes shown outside the carrier PCB area are optional, but it is recommended that all pods include the two mounting holes at the end of the board opposite the mezzanine connector. These mounting holes may be used for securing the board to a mechanical chassis or platform. Recommended hole locations are shown, but there are no restrictions on quantity, location, or size.

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3.1. Connectors

Standard pods and ports use a Samtec 40-pin QTE/QSE mating connector pair. The QTE/QSE series has a 0.8-mm pitch with equally spaced pins and a center ground spine.
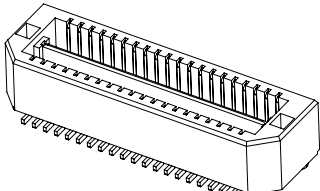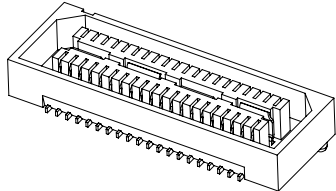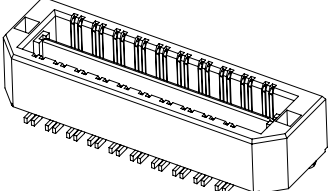
Transceiver pods and ports use a Samtec 40-pin QTH-DP/QSH-DP mating connector pair. The QTH-DP/QSH-DP series has a 0.5-mm pitch.
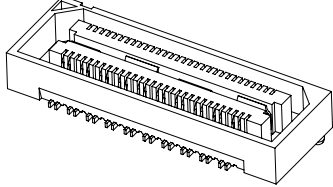
The QSE and QSH connectors (carrier-side) have only one option for height. The QTE and QTH connectors (pod-side) are available in several different heights to provide flexibility in board-to-board mating heights. The nominal mated height for an SYZYGY system is 5.00 mm. See the Samtec documentation for additional options.

All of the specified connectors have optional latching features to help maintain mechanical stability between pod and carrier. The non-latching versions of these connectors are technically compatible with the latching connector footprints, but it should be noted that latching and non-latching connectors do not mate together properly and therefore should not be intermixed. Furthermore, latching versions of the cables were not available at the time this specification was released. Therefore, it is recommend that carrier and peripheral vendors use the non-latching versions for broadest compatibility.

All ports and pods have the option for screw-down retention using the mounting holes on either side of the connector.

Table 7: Standard and Transceiver Connector Part Numbers

Device	Connector Part Number	Description
Standard Pod	Samtec QTE-020-xx-F-D-A xx = 01 for 5.00 mm nominal mated height See Samtec documentation for additional options.	High-speed ground place header terminal, 40-pin, 0.8-mm pitch
Standard Port	Samtec QSE-020-01-F-D-A	High-speed ground plane header socket, 40-pin, 0.8-mm pitch
Transceiver Pod	Samtec QTH-020-01-F-D-DP-A	High-speed ground plane header terminal, 40-pin, 0.5-mm pitch, differential pair spacing

Device	Connector Part Number	Description
Transceiver Port	Samtec QSH-020-01-F-D-DP-A	High-speed ground plane header socket, 40-pin, 0.5-mm pitch, differential pair spacing

3.1.1. Cables

In addition to direct board-to-board connection, a pod may also connect to a carrier via a cable. The Samtec EQCD cable series is compatible with the QSE/QTE connector series and is used for connecting a standard pod to a standard port. The Samtec HQDP cable series is compatible with the QSH-DP/QTH-DP connector series and is used for connecting a transceiver pod to a transceiver port. Both cable series are available in any custom length.

The part numbers in the table below specify a bottom-mount connector for the carrier termination and a top-mount connector for the pod termination. Other connector configurations are available. Refer to the applicable Samtec documentation for details.

**Table 8:** Standard and Transceiver Cable Part Numbers

Pod/Port	Cable Part Number	Description
Standard	Samtec EQCD-020-xx.xx-TBL-STL-1-B (xx.xx = cable length in inches)	0.8-mm pitch, 40-pin, bottom-side terminal connector (to carrier), top-side socket connector (to pod), pin 1 wired to pin 1, screw mount on both ends
Transceiver	Samtec HQDP-020-xx.xx-TBL-STL-1-B (xx.xx = cable length in inches)	0.5-mm pitch, 40-pin, bottom-side terminal connector (to carrier), top-side socket connector (to pod), pin 1 wired to pin 1, screw mount on both ends

xx.xx = cable length in inches

3.2. Standard Port Dimensions (Carrier)

The drawing below shows the dimensions of a standard port, including the location of the connector and mounting holes relative to the carrier PCB edge. In this top-down view, the connector is mounted on top of the carrier PCB, and the relative location of a standard pod is indicated by the dashed phantom line.

Note: The diagram below shows the recommended placement of a port on the carrier such that the peripheral hangs off the edge of the carrier. Non-edge placement of a port is allowed but carrier manufacturers should provide additional information to customers to help them evaluate peripheral compatibility.
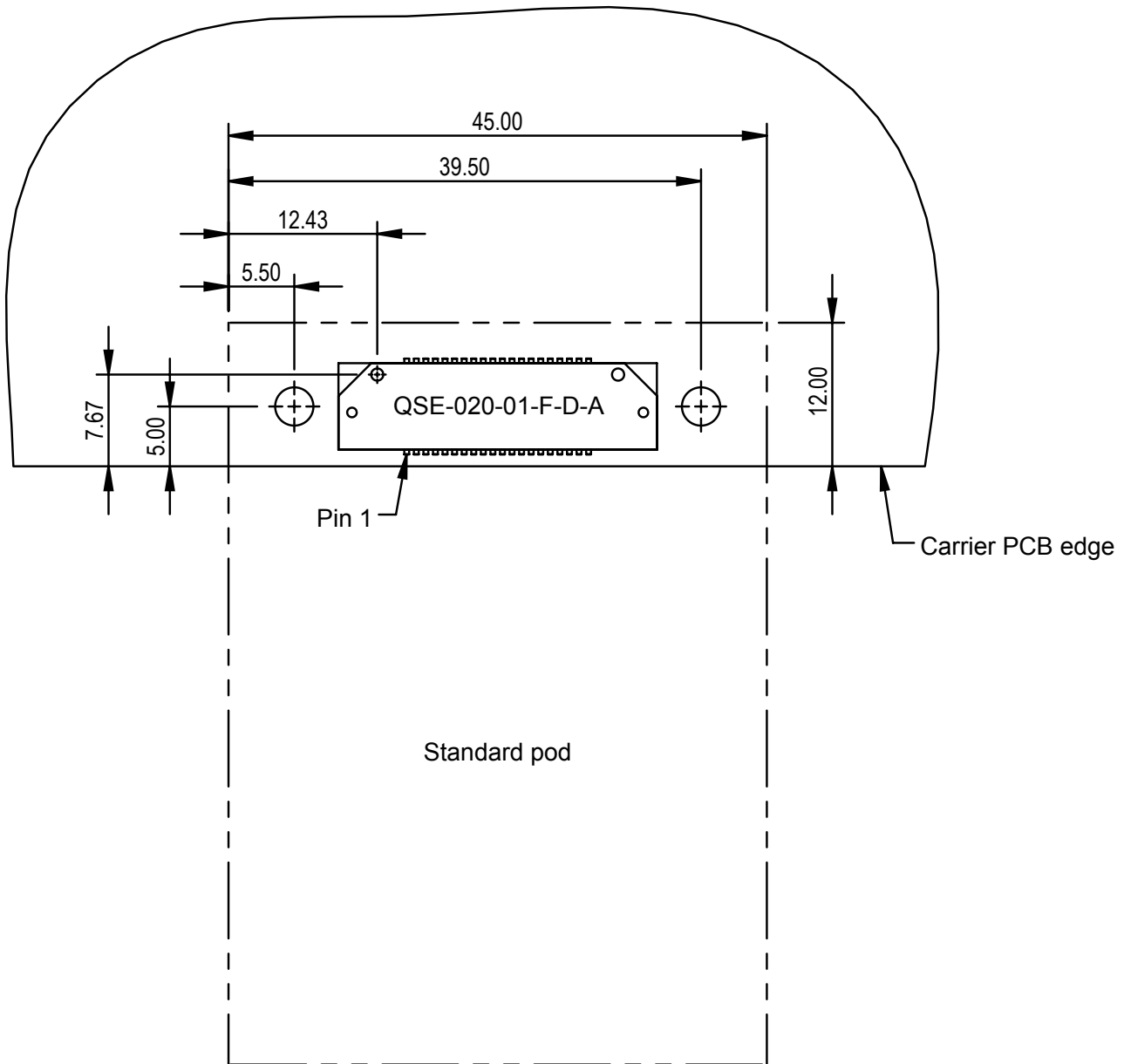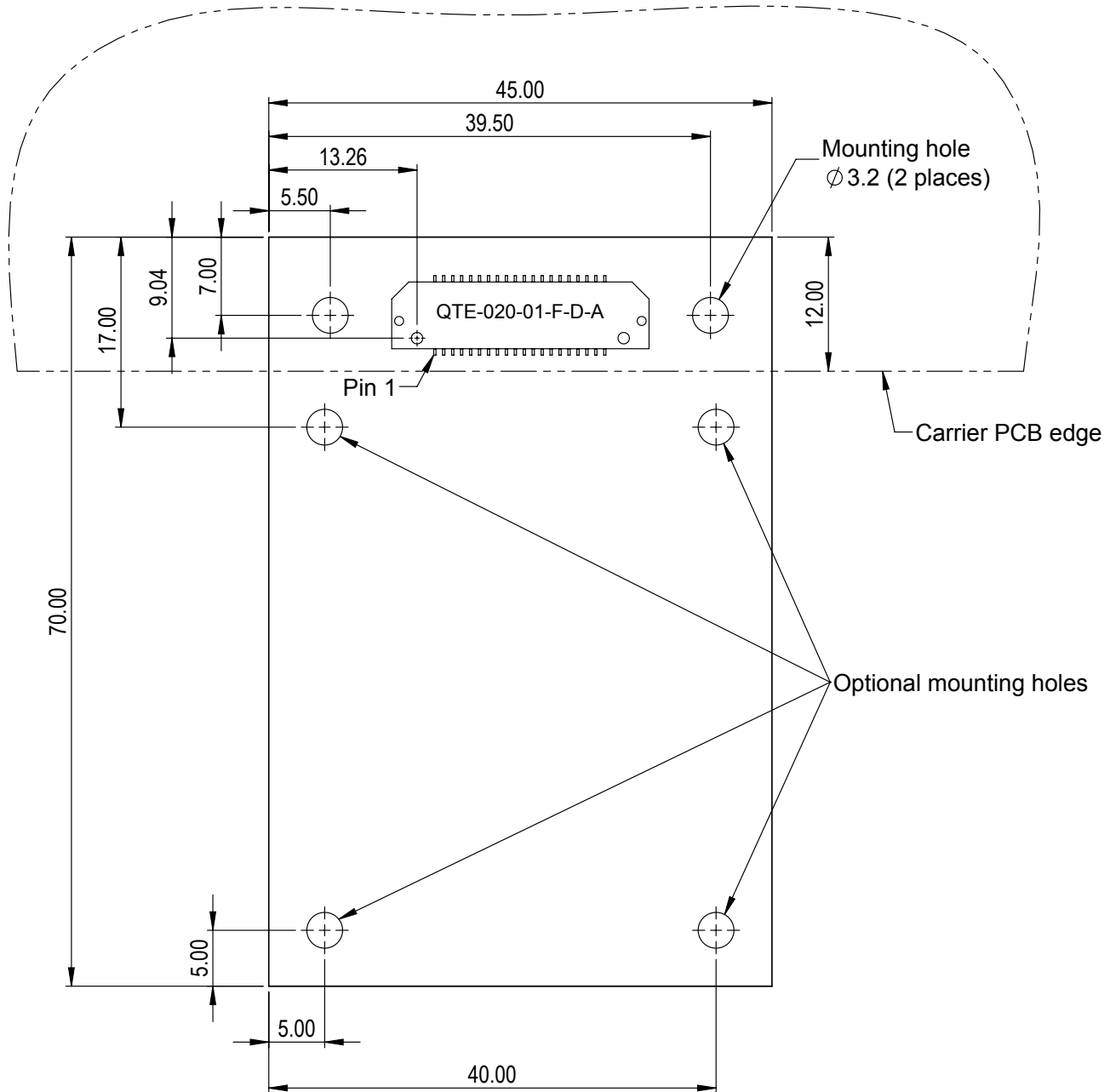

All dimensions in millimeters

Figure 3. Standard Port Dimensions

3.3. Standard Pod Dimensions

The drawing below shows the dimensions of a standard pod, including the location of the connector and mounting holes. In this top-down view, the connector is mounted on the bottom side of the pod PCB, and the relative location of the carrier PCB is indicated by the dashed phantom line.

Note: The peripheral length indicated in the figure (70 mm) is recommended. Depending on function and application, more suitable dimensions may be used. This dimension is not required by the standard.

All dimensions in millimeters

Figure 4. Standard Pod Dimensions

3.4. Transceiver Port Dimensions (Carrier)

The drawing below shows the dimensions of a transceiver port (both TXR-2 and TXR-4), including the location of the connector and mounting holes relative to the carrier PCB edge. In this top-down view, the connector is mounted on top of the carrier PCB, and the relative location of a transceiver pod is indicated by the dashed phantom line.

Note: The diagram below shows the recommended placement of a port on the carrier such that the peripheral hangs off the edge of the carrier. Non-edge placement of a port is allowed but carrier manufacturers should provide additional information to customers to help them evaluate peripheral compatibility.
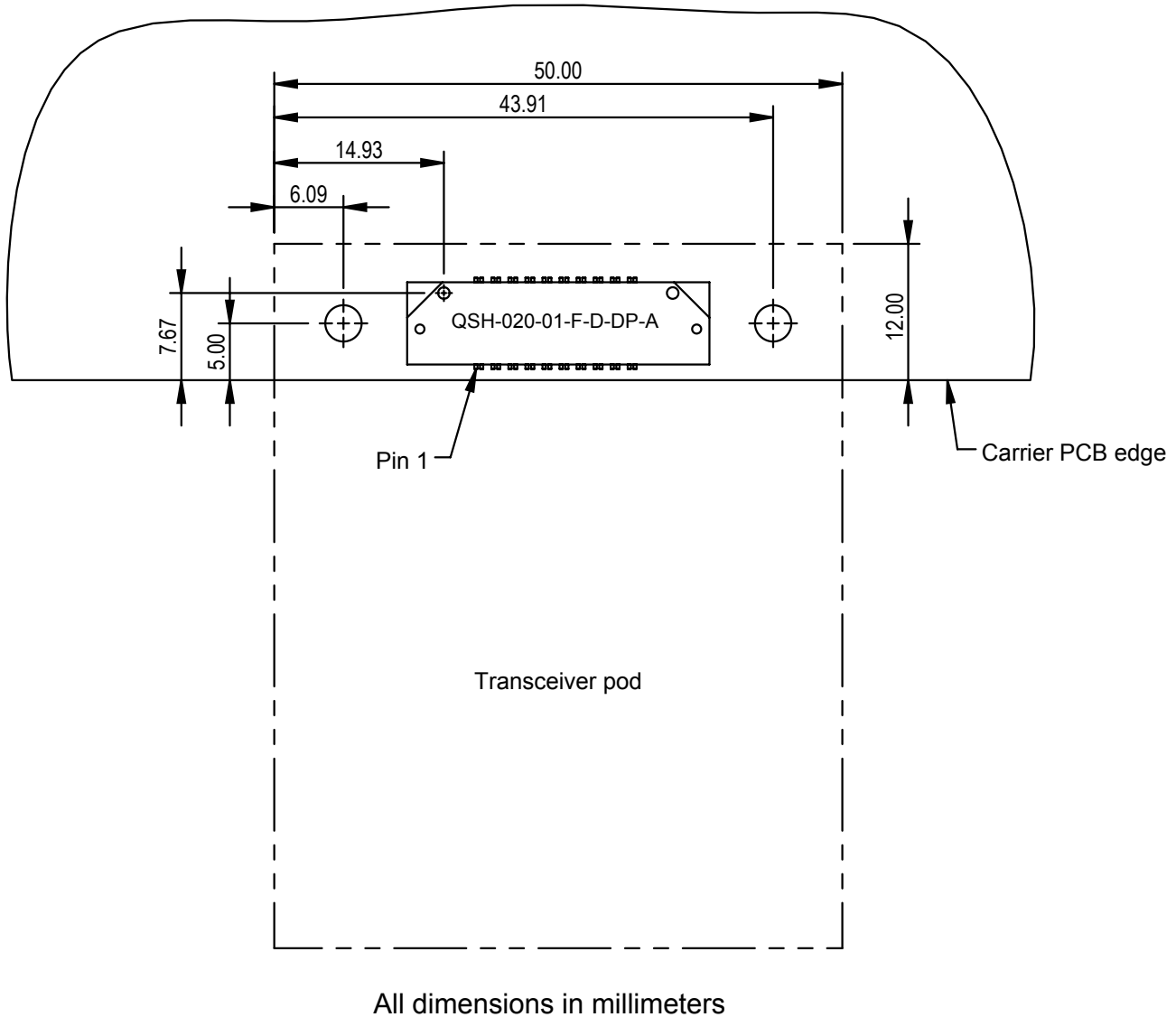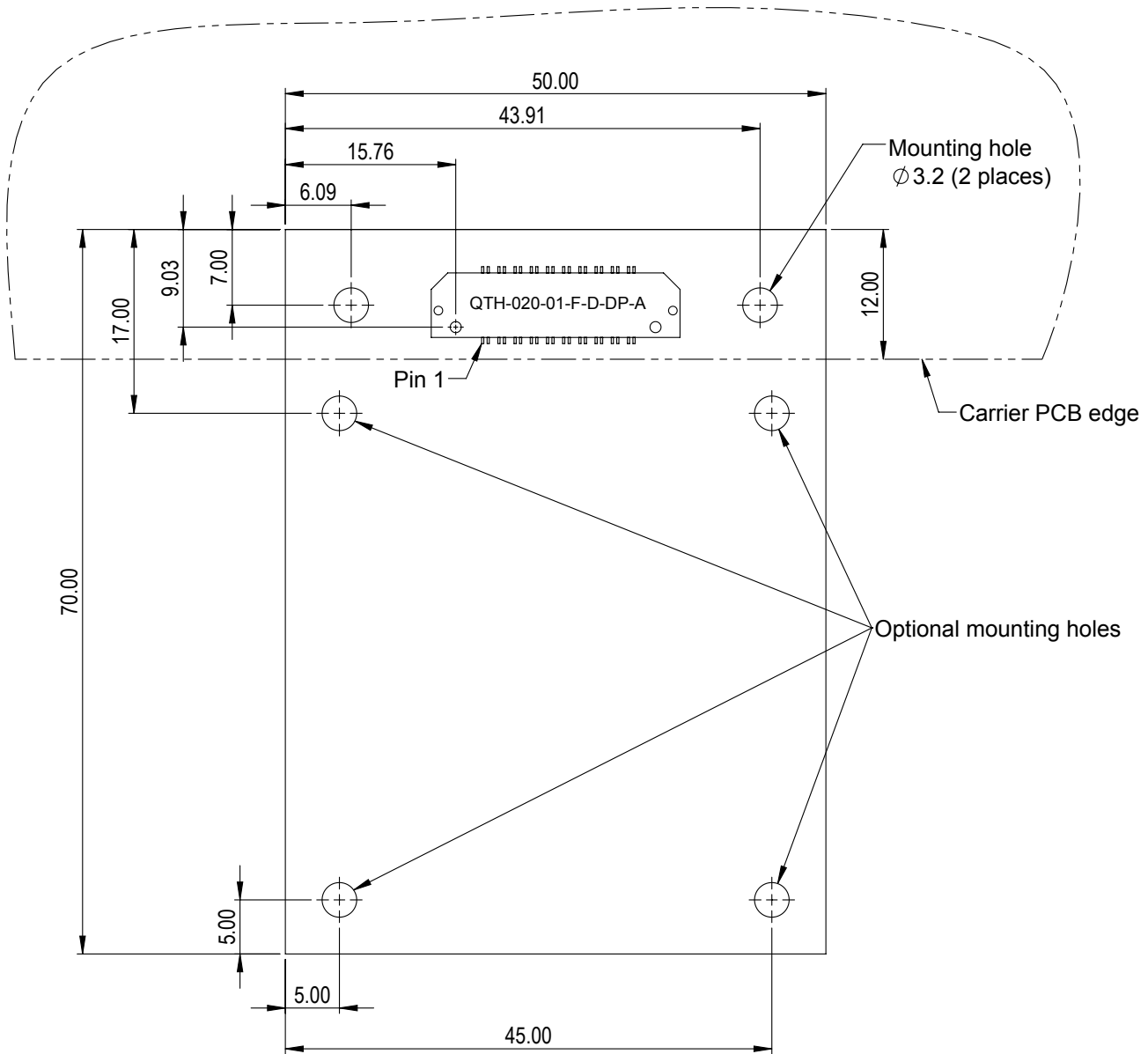
Figure 5. Transceiver Port Dimensions

3.5. Transceiver Pod Dimensions

The drawing below shows the dimensions of a transceiver pod (both TXR-2 and TXR-4), including the location of the connector and mounting holes. In this top-down view, the connector is mounted on the bottom side of the pod PCB, and the relative location of the carrier PCB is indicated by the dashed phantom line.

Note: The peripheral length indicated in the figure (70 mm) is recommended. Depending on function and application, more suitable dimensions may be used. This dimension is not required by the standard.

All dimensions in millimeters

Figure 6. Transceiver Pod Dimensions

3.6. Double-wide Pods

In order to accommodate peripherals which require more I/O than is available on a single port, a pod may use a "double-wide" configuration. A double-wide pod attaches to two adjacent ports of the same type on a carrier.

A carrier which accommodates double-wide pods must use a spacing of 2 mm between ports, measured from pod edge to pod edge. This is equivalent to a connector spacing of 47 mm for standard pods and 52 mm for transceiver pods.
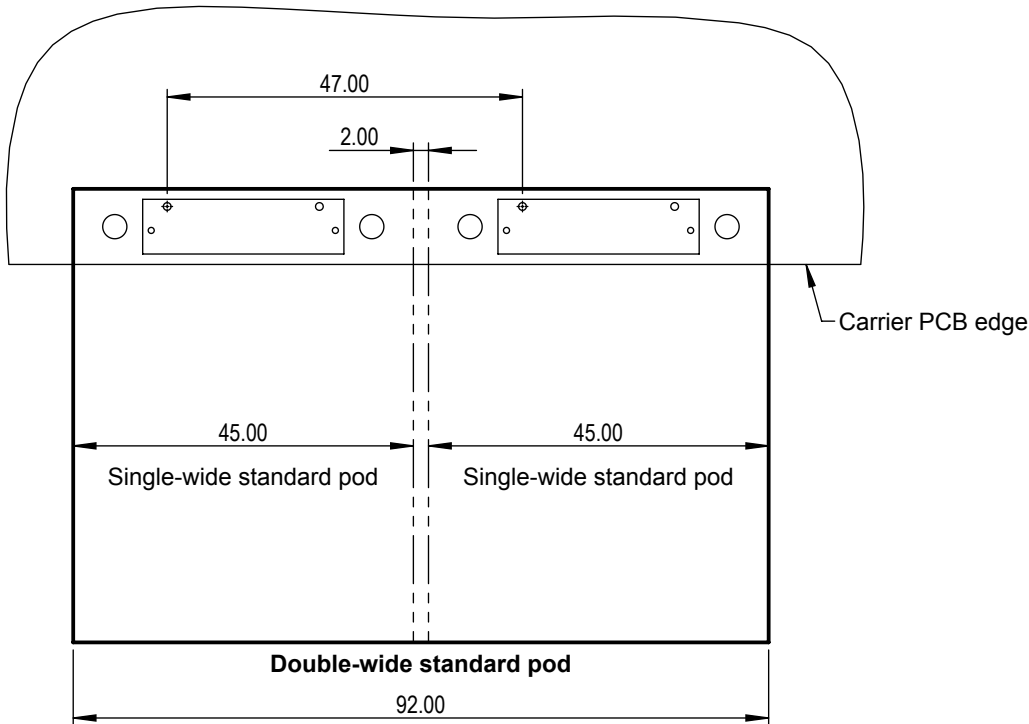

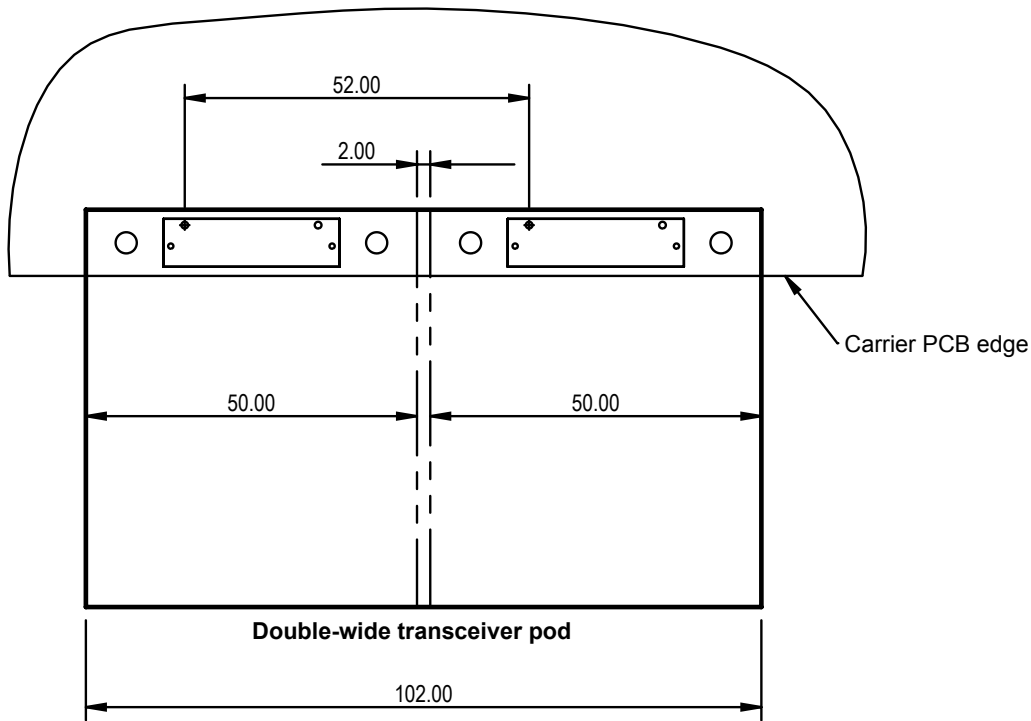**Figure 7.** Double-Wide Standard Pod Dimensions

Figure 8. Double-Wide Transceiver Pod Dimensions

3.7. Mechanical Integration with Other Systems

The SYZYGY specification does not provide any requirements or guidelines for integrating carriers and pods with other mechanical systems such as equipment chassis, front panels, cooling systems, etc.

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4. Electrical

4.1. Electrical Specifications

Table 9: SYZYGY Interface Electrical Specifications

Parameter	Specification	Notes
5V supply voltage	+5.0 VDC ±10%	This supply is required, provided by the carrier to the pods.
5V supply current	2 A max current draw per port; No requirement for minimum current provided by carrier.	Max pod current draw is limited by the max pin current supported by the Samtec mezzanine connector (2 A per pin). The total 5V current provided by the carrier shall be determined by the system designer according to the system parameters (number of ports, expected pod current draw, etc).
3.3V supply voltage	+3.3 VDC ±5%	This supply is required, provided by the carrier to pods.
3.3V supply current	2 A max current draw per port; No requirement for min/max current draw provided by carrier.	Max pod current draw is limited by the 2A pin current limit of the Samtec connector.
VIO supply voltage	Adjustable in 10 mV steps. No requirement for min/max range. ±5% for all voltages	It is recommended that carriers support a VIO range of at least 1.2V - 3.3V.
VIO supply current	2 A max current draw per port; No requirement for min/max current draw provided by carrier or pod.	The total VIO current provided by the carrier or pod shall be determined by the system designer according to the system parameters (number of ports, expected pod current draw, etc).

4.2. Power Supplies

An SYZYGY system includes three separate power supply domains: 5V, 3.3V, and VIO. All supply voltages are generated on the carrier and provided to the pods. There are no requirements for minimum current provided by any supply. The carrier designer should determine an appropriate current capability according to the relevant parameters of the design (total number of ports, expected pod current draw, etc). A pod is permitted to draw a maximum of 2 A from any power supply voltage. This is determined by the pin current limit of the mezzanine connector.

The 5V and 3.3V supplies may be shared across VIO groups.

4.2.1. VIO Supply

The VIO supply is required on the carrier. Each VIO group must have its own independently-configurable VIO supply. The VIO voltage for a VIO group is configured automatically at startup according to the hardware parameters communicated to the SmartVIO controller from all pods connected to that VIO group. If the pods within a

group do not share a common, compatible VIO voltage, the SmartVIO controller should keep the VIO voltage disabled for that group. The carrier may optionally allow user override of the VIO voltage.

4.3. Supply Sequencing

The carrier is required to implement the following power supply sequence:

1. 5V supply is enabled.
2. 3.3V supply is enabled at the same time as 5V or any time after (no timing requirement).
3. After 3.3V is within required regulation, the SmartVIO controller waits at least 100 ms and then queries all connected pods for personality information.
4. After all pods have been queried, the SmartVIO controller configures and enables the VIO supply (no timing requirement).

If a pod requires a specific power supply sequence that cannot be guaranteed by the sequence above, the pod must include the appropriate circuitry for gating and enabling supplies as required. The MCU may be used for this purpose.

4.4. Cable Deratings

The current ratings of the EQCD and HQDP cables are lower than the ratings for the associated mating connectors (QSE/QTE and QSH-DP/QTH-DP). The maximum recommended current per pin is shown in the table below.

Table 10: Suggested Maximum Current Derating for Samtec Cables

Cable	Maximum Current
EQCD	500 mA per pin
HQDP	400 mA per pin

The ratings in the above table are published by Samtec, based on a configuration using six adjacent pins powered simultaneously on the cable. To help with heat dissipation, the SYZYGY pinouts are designed to have physical separation between the power supply conductors (+5V, +3.3V, VIO). This may potentially allow higher maximum current per pin than is indicated in the table, but performance is not guaranteed.

Similarly, the maximum rated speeds of the cables are lower than that of the associated mating connectors. Samtec's published data is shown in the table below. For additional information, refer to the Samtec documentation.

Table 11: Suggested Maximum Speed Derating for Samtec Cables

Cable (Length)	Maximum Speed
EQCD (10")	5.50 GHz / 11.00 Gbps
HQDP (10")	9.50 GHz / 19.00 Gbps

5. SYZYGY DNA

Every peripheral includes an MCU (called the Peripheral MCU or pMCU) for storing its SYZYGY DNA, the characteristics which comprise a pod's "personality." This includes information about the peripheral's SmartVIO compatibility (current load and compatible VIO voltage range) as well as optional information such as manufacturer name, product name and model number, serial number, etc. The pMCU communicates over an I^2C bus with the SmartVIO controller. All pods connected to a carrier share a common I^2C bus.

The I^2C address of each pod is determined by a resistor divider formed between the carrier and the pod. A pull-down resistor R_GA is connected to each port on the carrier. Each port uses a unique resistor value. On the pod, a 10-kΩ pullup resistor is connected from R_GA to +3.3V. The R_GA net is connected to one of the pMCU ADC input pins, and the resulting voltage is used to determine the I^2C address of the pod. The recommended standard values for R_GA are shown in the **SYZYGY DNA Specification**. Resistor tolerance should be 1% or better.

The recommended pMCU is the Atmel ATtiny44A, an 8-bit RISC-based device with 4 KB of program memory and 256 bytes of data EEPROM.

The I^2C bus interfaces to the pods using 3.3V logic. Pull-up resistors for the SDA and SCL signals must be present on the carrier. If the I^2C interface to the SmartVIO controller operates at a logic voltage other than 3.3V, a bidirectional level translator such as the Texas Instruments PCA9306 may be used on the carrier.

Double-wide peripherals only need to include a single pMCU. This pMCU must be connected to the I^2C and R_GA lines from exactly one port. It follows that both ports on a double-wide peripheral must utilize a single VIO voltage and that the carrier treat the peripheral as though it has specified the same VIO on both ports.

Please see the separate **SYZYGY DNA Specification** document for more information about the features, functionality, and implementation of carrier- and peripheral-side SYZYGY DNA support.

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7. Appendix A: SYZYGY Compatibility Tables

The documentation for a SYZYGY device should include a table which outlines the compatibility and interoperability with other SYZYGY devices. This information can be helpful to consumers to determine carrier and pod compatibility.

Table 12: Example Carrier Compatibility Table

Parameter	Port A	Port B	Port C	Port D
Total 5V Supply Current	2.5 A (shared with USB +5V output)			
Total 3.3V Supply Current	2 A shared (Ports A and B)		2 A shared (Ports C and D)	
VIO Supply Voltage Range	1.2 - 3.3 V			
Total VIO Supply Surrent	4 A (VIO Group 1)		4 A (VIO Group 2)	
Port Type	Standard	Transceiver (TXR-2)	Standard	Standard
	Single-Wide	Single-Wide	Double-Wide Pair	
VIO Groups	Group 1: A, B		Group 2: C, D	
I/O Per Port	28 total (8 DP)	18 total	28 total (8 DP)	28 total (8 DP)
Length Matching	1557 - 2055 mils DP: 10 mils max within pair	1079 - 1578 mils Transceivers: 10 mils max within pair; 10 mils max pair-to-pair	2412 - 2505 mils DP: 10 mils max within pair	1220 - 1309 mils DP: 10 mils max within pair

Table 13: Example Pod Compatibility Table

Parameter	Example
Type	SYZYGY Standard
Maximum 5V supply current	500 mA
Maximum 3.3V supply current	250 mA
VIO supply voltage(s)	1.8 V, 2.5 V, or 3.3 V
Maximum VIO supply current	100 mA
Total number of I/O	12
Number of differential I/O pairs (Standard pod only)	4
Width	Single